CLAIMS:

1. A cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously or alternately causing an etching agent having an etching action with respect to the semiconductor layer and crystal growth source material to come into contact with the semiconductor layer.

2. A cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of exposing the surface of the semiconductor layer to an atmosphere containing an etching agent having an etching action with respect to the semiconductor layer and crystal growth source material.

3. A cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously providing a first gas including an etching agent having an etching action with respect to the semiconductor layer and a second gas including crystal growth source material to the surface

of the semiconductor layer.

4. The cleaning treatment method according to claim 3, wherein the first gas and the second gas are supplied in an intermittent manner.

5. The cleaning treatment method according to any one of claims 1 to 4, wherein a difference in layer thickness of the semiconductor layer before and after implementation of the cleaning treatment step is 100 nm or less.

6. The cleaning treatment method according to any one of claims 1 to 5, wherein layer thickness of the semiconductor layer is not substantially reduced during implementation of the cleaning treatment step.

7. The cleaning treatment method according to claim 5 or 6, wherein change in layer thickness of the semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material.

8. The cleaning treatment method according to claim 3 or 4, wherein when it is taken that: a symbol for rate of change of layer thickness of the semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases;

rate of change of layer thickness of the

semiconductor layer during implementation of the cleaning treatment step is R;

rate of change of layer thickness of the semiconductor layer in the case of supplying only the first gas to the semiconductor layer surface is r_1, and

rate of change of layer thickness of the semiconductor layer in the case of supplying only the second gas to the semiconductor layer surface is r_2,

the amount of the first gas and the second gas supplied is adjusted in such a manner that

an absolute value for the rate of change of layer thickness becomes:

$|R| < |r_2| < |r_1|$

9. The cleaning treatment method according to claim 8, wherein $R < 0$.

10. The cleaning treatment method according to claim 8 or 9, wherein

$|R|$ is 0.1 nm/sec or less.

11. The cleaning treatment method according to any one of claims 1 to 10, wherein the crystal growth source material includes an element constituting the semiconductor layer.

12. The cleaning treatment method according to any one of claims 1 to 11, wherein the crystal growth source material

includes organic metal.

13. The cleaning treatment method according to any one of claims 1 to 12, wherein the etching agent is a halogen element or compound thereof.

14. The cleaning treatment method according to any one of claims 1 to 13, wherein the semiconductor layer is comprised of compound semiconductor.

15. The cleaning treatment method according to claim 14, wherein the semiconductor layer is comprised of a group III - V compound semiconductor.

16. The cleaning treatment method according to claim 15, wherein the crystal growth source material is a compound including a group III element constituting the semiconductor layer.

17. The cleaning treatment method according to claim 15 or 16, wherein the group III element constituting the semiconductor layer is comprised of a single species.

18. The cleaning treatment method according to any one of claims 15 to 17, wherein the group III element constituting the semiconductor layer is indium (In).

19. A method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer at an upper part of a semiconductor substrate;

subjecting the surface of the first semiconductor layer to cleaning treatment; and

forming a second semiconductor layer on the first semiconductor layer,

wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of causing an etching agent having an etching action with respect to the semiconductor layer and crystal growth source material to come into contact with the surface of the semiconductor layer.

20. A method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer at an upper part of a semiconductor substrate;

subjecting the surface of the first semiconductor layer to cleaning treatment; and

forming a second semiconductor layer on the first semiconductor layer,

wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of exposing the surface of the semiconductor layer to an atmosphere containing an etching agent having an etching

action with respect to the semiconductor layer and crystal growth source material.

21. A method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer at an upper part of a semiconductor substrate;

subjecting the surface of the first semiconductor layer to cleaning treatment; and

forming a second semiconductor layer on the first semiconductor layer,

wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of simultaneously supplying a first gas including an etching agent having an etching action with respect to the semiconductor layer and a second gas including crystal growth source material to the surface of the semiconductor layer.

22. The method of manufacturing a semiconductor device according to claim 21, wherein the first gas and the second gas are supplied in an intermittent manner.

23. The method of manufacturing a semiconductor device according to any one of claims 19 to 22, wherein a difference in layer thickness of the second semiconductor layer before and after implementation of the step of

subjecting the surface of the first semiconductor layer to cleaning treatment is 100 nm or less.

24. The method of manufacturing a semiconductor device according to any one of claims 19 to 23, wherein layer thickness of the second semiconductor layer is not substantially reduced during implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment.

25. The method of manufacturing a semiconductor device according to claim 23 or 24, wherein change in layer thickness of the first semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material.

26. The method of manufacturing a semiconductor device according to claim 21 or 22,
wherein when it is taken that:

a symbol for rate of change of layer thickness of the first semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases;

rate of change of layer thickness of the first semiconductor layer during implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment is R;

rate of change of layer thickness of the first

semiconductor layer in the case of supplying only the first gas to the first semiconductor layer surface is r1, and

rate of change of layer thickness of the first semiconductor layer in the case of supplying only the second gas to the first semiconductor layer surface is r2,

the amount of the first gas and the second gas supplied is adjusted in such a manner that

an absolute value for the rate of change of layer thickness becomes:

$$|R| < |r_2| < |r_1|$$

27. The method of manufacturing a semiconductor device according to claim 26, wherein $R < 0$.

28. The method of manufacturing a semiconductor device according to claim 26 or 27, wherein $|R|$ is 0.1 nm/sec or less.

29. The method of manufacturing a semiconductor device according to any one of claims 19 to 28, wherein the crystal growth source material includes an element constituting the first semiconductor layer.

30. The method of manufacturing a semiconductor device according to any one of claims 19 to 29, wherein the crystal growth source material includes a metal organic.

31. The method of manufacturing a semiconductor device according to any one of claims 19 to 30, wherein the etching agent is a halogen element or compound thereof.

32. The method of manufacturing a semiconductor device according to any one of claims 19 to 31, wherein the first semiconductor layer is comprised of compound semiconductor.

33. The method of manufacturing a semiconductor device according to claim 32, wherein the first semiconductor layer is comprised of compound semiconductor.

34. The method of manufacturing a semiconductor device according to claim 33, wherein the crystal growth source material includes a group III element constituting the first semiconductor layer.

35. The method of manufacturing a semiconductor device according to claim 34, wherein the group III element constituting the semiconductor layer is a single species.

36. The method of manufacturing a semiconductor device according to claim 35, wherein the group III element constituting the semiconductor layer is indium (In).

37. The method of manufacturing a semiconductor device according to any one of claims 19 to 36, wherein the first

semiconductor layer and the second semiconductor layer are formed using vapor phase epitaxy.

38. The method of manufacturing a semiconductor device according to any one of claims 19 to 37, wherein a mask is formed on the first semiconductor layer after the step of forming the first semiconductor layer, and after eliminating the mask, the step of subjecting the surface of the first semiconductor layer to cleaning treatment is implemented.

39. An optical semiconductor device with a concentration of residual Si of a regrowth interface within a p-type semiconductor layer having a surface density of 5×10^{11} atoms/cm^2 or less.

40. The optical semiconductor device according to claim 39, wherein the regrowth interface is an interface of a p-type current block layer and a layer connecting with a lower part of the p-type current block layer.

41. The optical semiconductor device according to claim 39, wherein the regrowth interface is an interface of a p-type cladding layer and a layer connecting with a lower part of the p-type cladding layer.

42. The optical semiconductor device according to claim

39, wherein the regrowth interface is a regrowth interface within a p-type cladding layer.

43. The optical semiconductor device according to any one of claims 39 to 42, having an active MMI structure.

44. An optical semiconductor integrated device with a concentration of residual Si of a regrowth interface within a p-type semiconductor layer having a surface density of 5 x 10^{11} atoms/cm^2 or less.

45. The optical semiconductor integrated device according to claim 44, wherein the regrowth interface is an interface of a p-type current block layer and a layer connecting with a lower part of the p-type current block layer.

46. The optical semiconductor integrated device according to claim 44, wherein the regrowth interface is an interface of a p-type cladding layer and a layer connecting with a lower part of the p-type cladding layer.

47. The optical semiconductor integrated device according to claim 44, wherein the regrowth interface is a regrowth interface within a p-type cladding layer.

48. The optical semiconductor integrated device according to any one of claims 44 to 47, further having an active MMI

structure.